SPI Bus Communication CH Robotics UM6-LT IMU

Communicating with the UM6 via the SPI bus allows for much higher data rates and lower latency than would be available through the UART.
The UM6 SPI bus operates at a +3.3V logic level. The UM6 is a slave on the bus, remaining inactive unless queried by a master device. Since the SPI bus will not always be used, bus inputs (MOSI, SCK, SS) are pulled to +3.3V internally. This prevents noise from being registered by the UM6 as attempts to communicate with the sensor. While all SPI pins on the UM6 are +5V tolerant, interfacing with +5V devices may require level-shifting hardware or external pull-ups to allow the logic high output of the UM6 to register properly.

The UM6 SPI clock (SCK) is active low, with data clocked in on the first falling edge. The maximum clock rate is 400kHz. The master should place its data on the MOSI line on the clock falling edge.
All SPI operations begin when the master writes two control bytes to the bus. The first byte indicates whether the operation is a register read (0x00) or a write (0x01). The second byte is the address of the register being accessed.
A read operation is performed by writing the control byte 0x00 to the MOSI line, followed by the address of the register to be read. During the next four transfers, the UM6 will write the contents of the register to the MISO line starting with the most-significant byte in the register as shown in Figure 2 - Single Register Read Operation. The master should pull the MOSI line low during the remainder of the read.
A read operation can be extended to read more than one register at a time as shown in Figure 3 - Multiple Register Read Operation To initiate the batch read, the master should write the address of the next desired register to the MOSI line while last byte of the previous register is being transmitted by the UM6.
A write operation is performed by writing the control byte 0x01 to the MOSI line, followed by the address of the register to modify. During the next four transfers, the UM6 will read the data from the MOSI line and write it to the specified register. During a write operation, the UM6 will pull the MISO line low to indicate that it is receiving data. There is no batch write operation. The structure of a write operation is illustrated in Figure 4 - Single Register Write Operation.

Figure 1 - SPI Bus Timing

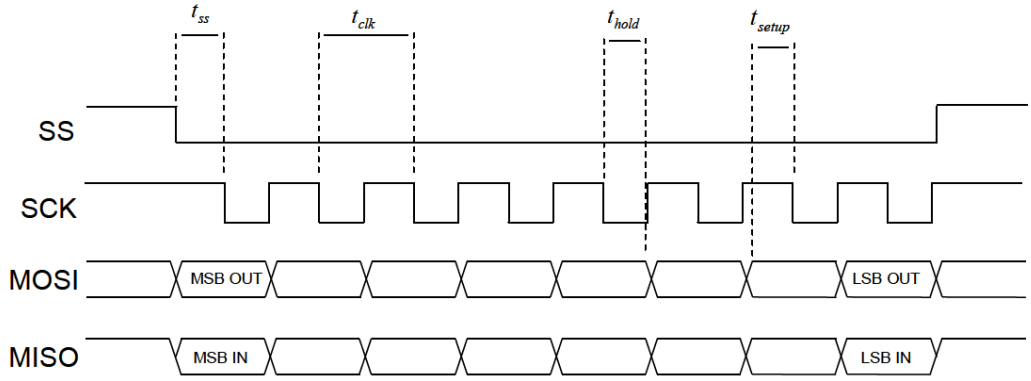

Table 13 - SPI Bus Timing

Name	Description	Min	Max
t_{ss}	Slave-select setup time	1 us	NA
t_{clk}	Clock period	2 us	5 us
f_{clk}	Clock frequency	200 kHz	500 kHz
t_{hold}	Data hold time	10 ns	NA
t_{setup}	Data setup time	10 ns	NA

Figure 2 - Single Register Read Operation

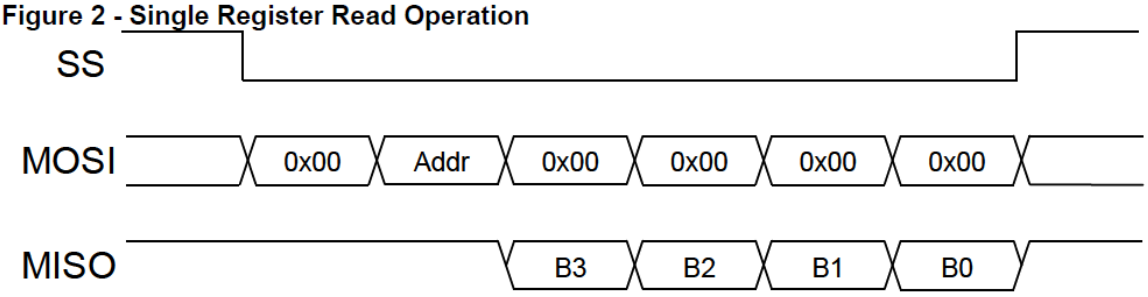

Figure 3 - Multiple Register Read Operation

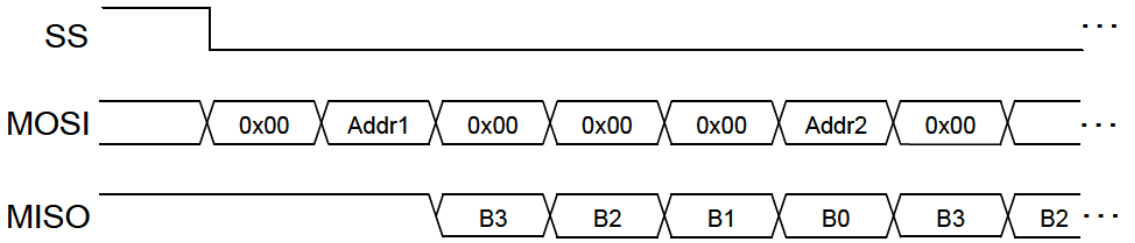

Figure 4 - Single Register Write Operation